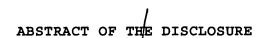
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An interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors is The interface includes an instruction bus and a provided. data bus. The instruction bus is configured to transfer instructions to the plurality of coprocessors instruction transfer order, where particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU. The data bus is configured to subsequently transfer the data. Data order signals within the data bus prescribe a data transfer order differs from the instruction transfer order that prescribing a transfer corresponding specific to outstanding particular instruction relative to all outstanding particular instructions.